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# APPARATUS FOR PARALLEL CALCULATION OF PREDICTION BITS IN A SPATIALLY PREDICTED CODED BLOCK PATTERN AND METHOD THEREOF

## Abstract

A storage device stores rows of bits including a D0 bit, an X0 bit, an X1 bit, a Y0 bit, a Y1 bit and a spatially predicted coded block pattern having an A0 bit, an A1 bit, an A2 bit, and an A3 bit. A first circuitis connected to the storage device for setting the A0 bit. A second circuitis connected to the storage device for setting the A2 bit and operates in parallel to the first circuit. In a second clock cycle, the bits in the storage device are shifted and the first circuit and the second circuit are reused to calculate the A1 bit and the A2 bit in parallel. Alternatively, a third circuit and a fourth circuit can be connected to the storage device to calculate the A1 bit and the A2 bit in parallel during the first clock cycle.